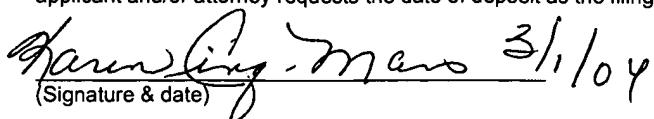


I hereby certify that this correspondence is being deposited with the United States Postal Service via Express Mail Certificate No.: ER046066445US1 addressed to : Commissioner of Patents and Trademarks, Alexandria, VA 22313, on March 1, 2004. The applicant and/or attorney requests the date of deposit as the filing date. Depositor: Karen Cinq-Mars

  
(Signature & date) 3/1/04

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of \_\_\_\_\_: March 1, 2004  
Dureseti Chidambarao, et al.: Group Art Unit:  
Serial No. to be assigned \_\_\_\_\_: Examiner: to be assigned  
Filed: 3/1/04 \_\_\_\_\_: International Business Machines Corporation  
2070 Route 52  
Hopewell Junction, NY 12533

TITLE: METHOD AND MANUFACTURE OF FINFET DEVICES WITH T-SHAPED FINS AND  
DEVICES MANUFACTURED THEREBY

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

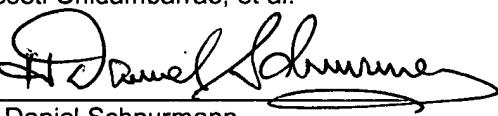
Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,  
Dureseti Chidambarao, et al.

By   
H. Daniel Schnurmann  
Registration No. 35,791  
Telephone No. 845-894-2481

**PAGE 1 OF 2**

<b>FORM PTO-1449 (Modified)</b>		<b>Attorney Docket Number:</b> <b>FIS920030388US1</b>	<b>Serial Number</b>
<b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>		<b>APPLICANT: Omer Dokumaci et al.</b>	
<b>(Use several sheets if necessary)</b>		<b>Filing Date:</b>	<b>Group:</b>

<b>Examiner Initials</b>	<b>Document Number</b>	<b>Issued Date</b>	<b>Name</b>	<b>Class</b>	<b>Subclass</b>	<b>FILING DATE (IF APPRO.)</b>
AA	6,252,284	26 Jun. 2001	Muller et al.	274	412	
AB	6,352,872	5 Mar. 2002	Kim et al.	438	24	
AC	6,391,695	21 May 2002	Yu	438	166	
AD	6,413,802	2 Jul. 2002	Hu et al.	438	151	
AE	6,429,061	6 Aug. 2002	Rim	438	198	
AF	6,433,609	13 Aug. 2002.	Voldman	327	313	
AG	6,583,015	24 Jun. 2003	Fitzgerald	438	287	
AH	6,583,469	24 Jun. 2003	Fried et al.	257	329	
AI	6,603,156	5 Aug. 2003	Rim	257	190	
AJ	6,610,576	26 Aug. 2003	Nowak	438	301	
AK	6,611,029	26 Aug. 2003	Ahmed et al.	257	365	
AL	6,635,909	21 Oct. 2003	Clark et al.	257	192	
AM	6,642,090	4 Nov. 2003	Fried et al.	438	164	
AO	6,642,536	4 Nov. 2003	Xiang et al.	257	19	
AP	6,657,252	2 Dec. 2003	Fried et al.	257	316	
AQ	6,657,259	2 Dec. 2003	Fried et al.	257	350	
AR	6,662,350	9 Dec. 2003	Fried et al.	716	11	
AS	6,664,582	16 Dec. 2003	Fried et al.	257	308	

**EXAMINER****DATE CONSIDERED**

**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

**PAGE 2 OF 2**

<b>FORM PTO-1449 (Modified)</b>		<b>Attorney Docket Number:</b> <b>FIS920030388US1</b>	<b>Serial Number</b>
<b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>  <b>(Use several sheets if necessary)</b>		<b>APPLICANT: Omer Dokumaci et al.</b>	
		<b>Filing Date:</b>	<b>Group:</b>

		<b>Published Application No.</b>	<b>Publication Date</b>	<b>Name</b>	<b>Class</b>	<b>Subclass</b>	
	AT	2003 0227036	11 Dec. 2003	Sugiyama et al.	257	288	
	AU	2004 0007715	15 Jan. 2004	Webb et al.	257	192	

**OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)**

	AX	Wong et al. "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25nm Thick Silicon Channel, IEDM pp 97-427 to 430, pp. 16.6.1-16.6.4", 1997 IEEE
	AW	Leobandung et al. "Wire-channel and Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors with a Significant Reduction of Short Channel Effects", J. Vac. Sci Technol. B 15 (6), Nov/Dec 1997 American Vacuum Society , pp. 2791-2794
	AX	Huang et al. "Sub 50-nm FinFET: PMOS" 1999 IEEE, IEDM 99-67 to 70, pp 3.4.1 to 3.4.4, 1999 IEEE
	AY	Huang et al. "Sub 50-nm FinFET" IEEE Transactions on Electron Devices, Vol. 48, No. 5 May 2001, pp 880-886, 2001 IEEE
	AZ	Tezuka et al. "High-performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique", 2002 Symposium On VLSI Technology Digest of Technical Papers, 10.3, pp. 96-97, 2002 IEEE

<b>EXAMINER</b>	<b>DATE CONSIDERED</b>
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